

DOCKET NO. REYNICK 2

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Joseph A. Reynick

Serial No.: N/A

Filed: Herewith

For: INTEGRATED CIRCUIT EARLY LIFE FAILURE DETECTION  
BY MONITORING CHANGES IN CURRENT SIGNATURES

Group No.: N/A

Examiner: N/A

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

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INFORMATION DISCLOSURE STATEMENT

Pursuant to the duty of disclosure under 37 C.F.R. § 1.56, Applicant submits this statement.

This submittal is made in accordance with 37 C.F.R. §§ 1.97 and 1.98 and § 609 of the Manual of Patent Examining Procedure. The patents, publications and other information herein are listed below and on the attached Form PTO-1449. Copies of the listed references are submitted herewith.

U.S. Patent No.  
6,140,832  
5,889,408

Inventor  
Vu et al.  
Miller

Date  
October 31, 2000  
March 30, 1999

**BEST AVAILABLE COPY**

Reference:

Parent application Serial No. 09/558,130 filed on April 25, 2000 to Joseph A. Reynick, entitled "INTEGRATED CIRCUIT EARLY LIFE FAILURE DETECTION BY MONITORING CHANGES IN CURRENT SIGNATURES"; allowed November 12, 2003.

Thibeault, "A NOVEL PROBABILISTIC APPROACH FOR IC DIAGNOSIS BASED ON DIFFERENTIAL QUIESCENT CURRENT SIGNATURES", 15th IEEE VLSI Test Symposium, 27 April-1 May 1997, pp. 80-85.

Thibeault et al. "DIAGNOSIS METHOD BASED ON DELTA-IDDQ PROBABILISTIC SIGNATURES: EXPERIMENTAL RESULTS"; IEEE International Test Conference, 1998 (Month Unavailable), pp. 1019-1026.

Thibeault, "ON THE COMPARISON OF DELTA-IDDQ AND IDDQ TESTING," VLSI Test Symposium, 17th IEEE Proceedings, 25-29 April 1999, pp. 143-150.

Thibeault, "IMPROVING DELTA-IDDQ-BASED TEST METHODS", IEEE International Test Conference Proceedings, 3-5 Oct. 2000; pp. 207-206.

Applicant hereby expressly reserves the right to swear behind the effective dates of any of the above Patents and to question the relevance and materiality of the Patents and Publications listed herein, in whole, in part, or in combination, subsequent to filing this Information Disclosure Statement.

Respectfully submitted,

HITT GAINES, P.C.



Charles W. Gaines

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**Complete if Known**

*(Use as many sheets as necessary)*

Sheet	1	of	2
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Application Number	N/A
Filing Date	Herewith
First Named Inventor	Joseph A. Reynick
Art Unit	N/A
Examiner Name	N/A
Attorney Docket Number	REYNICK 2

[illegible][illegible]Date  
Considered

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. <sup>1</sup> Applicant's unique citation designation number (optional). <sup>2</sup> See Kinds Codes of USPTO Patent Documents at [www.uspto.gov](http://www.uspto.gov) or MPEP 901.04. <sup>3</sup> Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). <sup>4</sup> For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. <sup>5</sup> Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. <sup>6</sup> Applicant is to place a check mark here if English language. Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND**

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Substitute for form 1449/PTO  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  <i>(Use as many sheets as necessary)</i>				<b>Complete if Known</b>	
				Application Number	N/A
				Filing Date	Herewith
				First Named Inventor	Joseph A. Reynick
				Art Unit	N/A
				Examiner Name	N/A
Sheet	2	of	2	Attorney Docket Number	REYNICK 2

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		Parent application Serial No. 09/558,130 filed on April 25, 2000 to Joseph A. Reynick, entitled "INTEGRATED CIRCUIT EARLY LIFE FAILURE DETECTION BY MONITORING CHANGES IN CURRENT SIGNATURES"; allowed November 12, 2003.	
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<sup>1</sup> Applicant's unique citation designation number (optional). <sup>2</sup> Applicant is to place a check mark here if English language Translation is attached.

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